XJTAG DFT Assistant

Overview

Accessing the power of Boundary Scan through JTAG-compliant ICs provides many benefits during prototype bring-up and in production test. The XJTAG® DFT Assistant for Altium Designer® performs the checks needed to ensure your JTAG chain is right first time, by design.

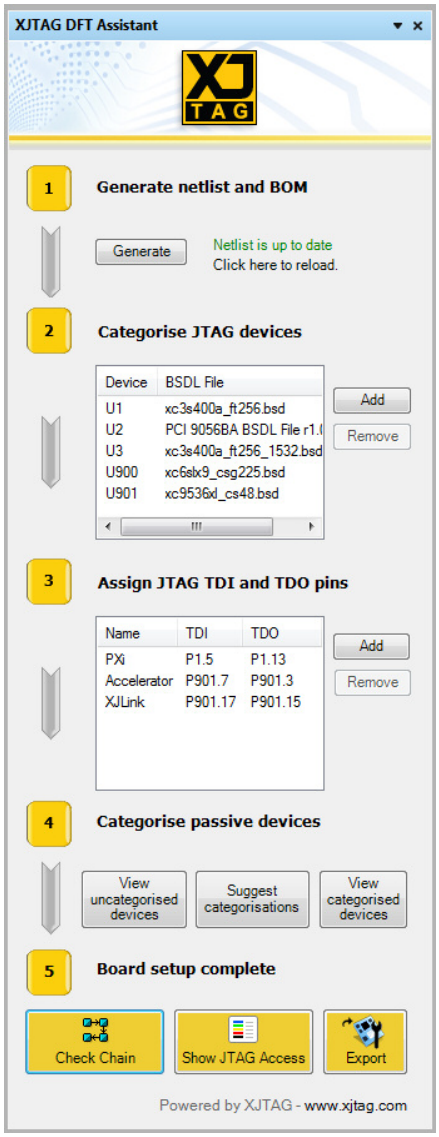
Key Benefits

- Carry out a DFT analysis for Boundary Scan access from within Altium Designer
- Avoid errors early in the development cycle, reducing PCB re-spins or modifications
- Understand where your JTAG chain provides test access through colour-coded views
- Extend your Boundary Scan test coverage by correctly implementing JTAG chains
- Improve the production process and reduce your time-to-market
- Export all data to XJDeveloper (Full or Evaluation Licence for XJTAG tools required)

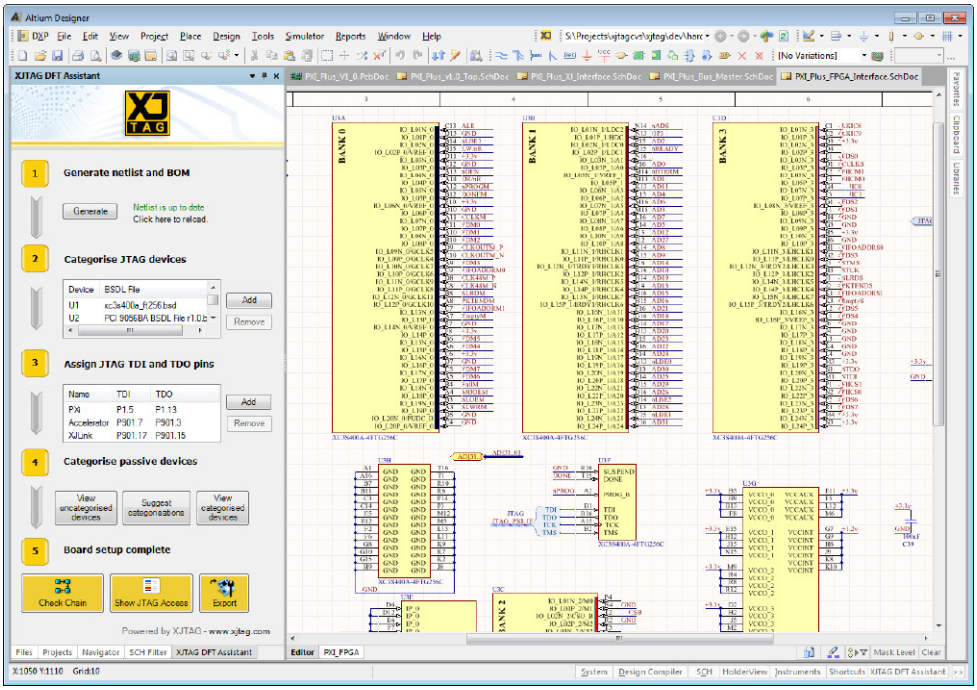
Right by Design

Implementing a JTAG chain in your PCB requires compliance with Design for Test (DFT) best practices. Making full use of this powerful technology available in most modern, highly functional ICs such as Microprocessors, Microcontrollers, DSPs and FPGAs relies on all JTAG chains being connected correctly and properly terminated. Seeing how much of your PCB can be accessed using Boundary Scan is also beneficial, as it provides developers with the information they need in order to design for maximum test coverage.

The XJTAG DFT Assistant helps automate this process. The Assistant associates imported BSDL files with their relevant components on the schematic, providing the Extension with the information it needs to understand the JTAG chain. Logic and passive devices that propagate a Boundary Scan chain can also be identified and categorised, enabling complete chains on the schematic to be checked for correctness. By visualising the extent of JTAG access, developers can easily see how much of their design can be accessed, and how coverage could be extended to include parts of a design not accessible to boundary scan testing.



The XJTAG DFT Assistant for Altium Designer Software Extension docks in the design view and is active during schematic design, to run chain checks or view Boundary Scan access at any time during the development process



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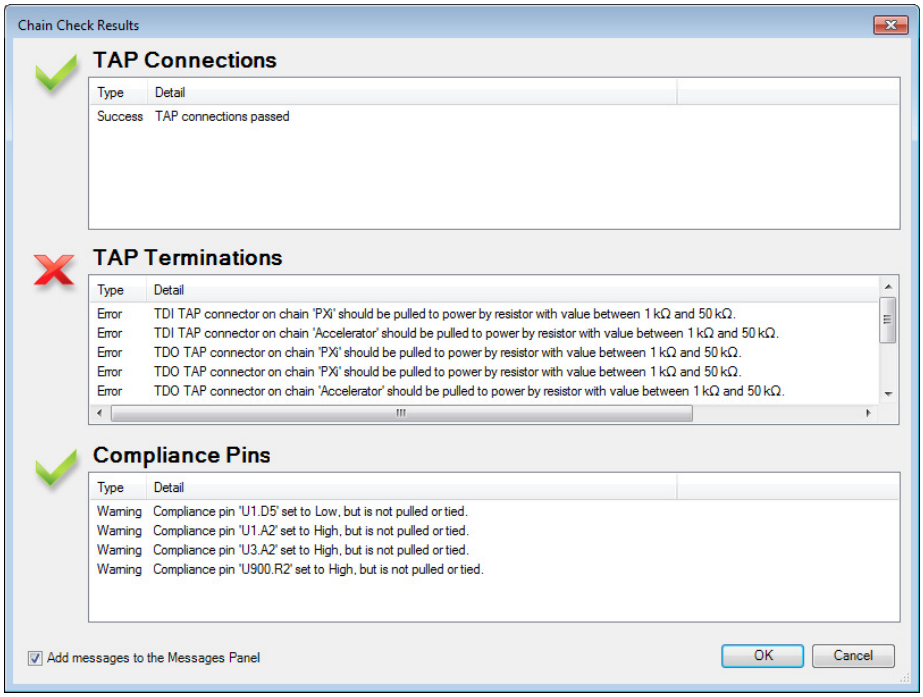


The XJTAG Chain Checker identifies and categorises faults and warnings in the boundary scan chain(s)

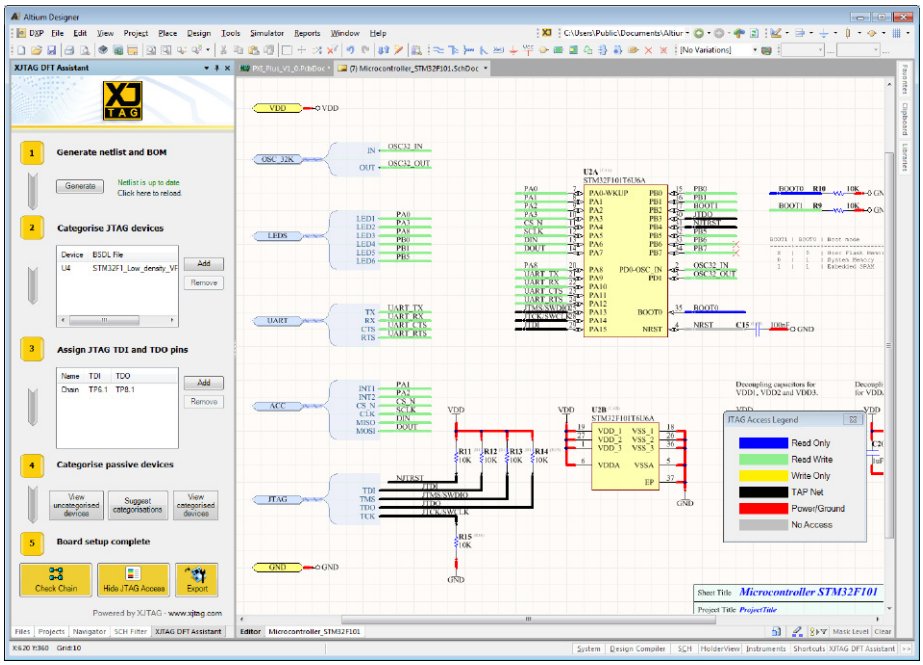
Installing XJTAG DFT Assistant for Altium Designer means developers will be able to find and correct potential problems in a JTAG chain before moving to layout, saving time and cost in their overall project.

Further Details:

The XJTAG DFT Assistant for Altium Designer software extension comprises the XJTAG Chain Checker and the XJTAG Access Viewer.

The Chain Checker tool works by analysing the netlist and finding a routable scan chain. It identifies errors and gives warnings of potential problems found on JTAG chains, including:

- Connection errors if any of the JTAG Test Access Point (TAP) signals are connected to the wrong pin(s) on a JTAG-compliant IC.
- Termination warnings if any of the TAP signals are not terminated as recommended.
- Compliance pin errors if they are incorrectly pulled high or low, or are left floating.



The XJTAG Access Viewer provides a clear indication of test access at any point during design

Features

- Fully assisted board setup to carry out a JTAG DFT analysis
- Automatic import of netlist from Altium Designer
- Includes a JTAG Access Viewer tool that highlights testable nets in a design on the schematic diagram
- Analysis of results from the Chain Checker tool clearly identify potential errors in the chain(s)
- Provides three categories of error: connection, termination and compliance
- Shows testable nets using colour-coded connections
- Assisted categorisation of non JTAG-enabled devices
- Export results to XJDeveloper for use in prototype bring-up and production test

The XJTAG DFT Assistant extension also identifies the extent of JTAG access across an entire schematic. This is overlaid on to the schematic using the XJTAG Access Viewer, allowing designers to understand their test access at an early stage in the design. By visualising the extent of test access, engineers are able to see the impact design changes have on their board's testability, watching it increase as additional nets on the board are made accessible to Boundary Scan.

The entire process of DFT analysis is handled by the extension and reported back within Altium Designer. The information gathered can also be exported as an XJDeveloper project, where it can be imported and used as the basis for further test development, using an XJLink/XJLink2 controller for testing the PCB once it has been manufactured.

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